A timer for ultra-low-power applications and variability in sub-threshold

Design Review

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Contents

1. Summary of papers

1.1. A 0.5 to 480 MHz self-referenced CMOS clock generator with 90 ppm total frequency Error and Spread spectrum Capability.

Quartz crystal based oscillators XOs operates at high speed and are power hungry. This paper presents a self-referenced CMOS LCO, or CMOS harmonic oscillator (CHO), that exhibits 90 ppm total frequency error over process, bias and temperature, thus making it suitable for replacing XOs in many applications. Additionally, the clock generator can be configured to produce a number of different output frequencies.

1.2. A Sub-pW timer using gate leakage for ultra low power sub-Hz monitoring systems. 2007

In general, crystal oscillators are used as reference for timer implementations. However these crystal oscillators operate at high frequencies and present high power consumption. This paper shows a circuit that takes advantage of gate leakage current to implement an ultra-low power watchdog timer. With this circuit, the voltage can rank from 0.3v to 1.2v It takes approximately ten minutes for the timer to reach steady state, after which the output frequency is always within 1% throughout the remaining 20 hours of testing. The RMS jitter for this timer is 30ms, equivalent to 0.14% of the output period.

1.3. A 150 pW Program and Hold Timer for Ultra Low Power Sensor Platforms. University of Michigan. 2009

This paper presents a program-and-hold timer with temperature self-compensation using a MOSFET gate leakage as the reference. At comparable power consumption, this system exhibits smaller temperature and supply sensitivity and a more technology portable design at the cost of silicon area.

1.4. A 660 pW Multi-Stage Temperature Compensated Timer for Ultra-Low-Power Wireless Sensor Node Synchronization. 2011

The gate leakage based timers achieves an acceptable power consumption <1nW. However it has high RMS jitter. This paper defines the uncertainty in a synchronization cycle of length T as a new metric SU. The timer period is a random variable with mean and sigma. The paper defines SU as the standard deviation of T. high RMS jitter is associated with high SU. To combat high SU the paper proposes : 1. A multistage structure with a high-gain triggering buffer, 2. Boosted Capacitance charging 3. The usage of a zero-threshold-voltage transistor for faster gate leakage discharge. 4. Closed loop temperature compensation to reduce temperature sensitivity.

1.5. A 2.60pJ/Inst Sub-threshold Sensor Processor for Optimal Energy Efficiency. 2006

This paper presents a sub-threshold sensor processor designed for energy efficiency at sub-threshold operation. In this paper, the author uses careful library selection and robust SRAM design enabled fully functional operation from 1.2V to 200 mV. It can be observed the relation between delay, frequency, VDD, dynamic energy, static energy and total energy.

1.6. Analysis and Mitigation of variability in sub threshold design

This paper considers how process variation takes effect in sub-threshold energy efficiency. The author shows how the variability can be addressed through circuit sizing and choice of circuit depth. In this paper they also show how the optimal VDD depends on process variation.

2. List of Activities and Chronogram

Date Start	Date Finish	Milestone	Activity	Done %
		Pre-Proposal Activities	Determine areas of interest	100
			Choose the project	100
			Look for publications	80
			Discuss with Professor	80
			Define the requirements	80
			Sketch the proposal	20
	4-Oct		Preliminar simulations	100
5-Oct	12-Oct	Proposal	Write Proposal	0
13-Oct	15-Oct	Develop Project	Choose circuit topology	20
16-Oct	19-Oct		Calculations	0
20-Oct	21-Oct		Draw the schematics	20
22-Oct	27-Oct		Run simulations	5
28-Oct	30-Oct		Draw the layout	0
31-Oct	1-Nov		Run DRC	0
2-Nov	3-Nov		Run LVC	0
10-Nov	16-Nov		Run Simulations including variation	0
17-Nov	-	Evaluation	Evaluate Performance	0
-	23-Nov		Make changes	0
24-Nov	3-Dic	Final Report	Write final report	0
4-Dec	4-Dec		Present Final Report	0

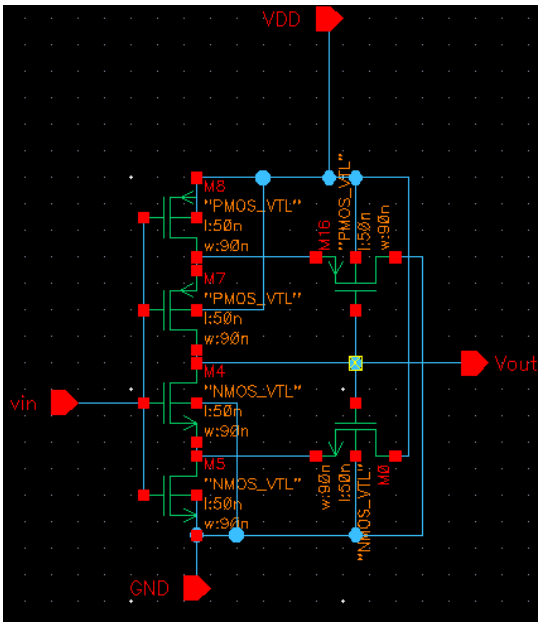
3. Advance of activities

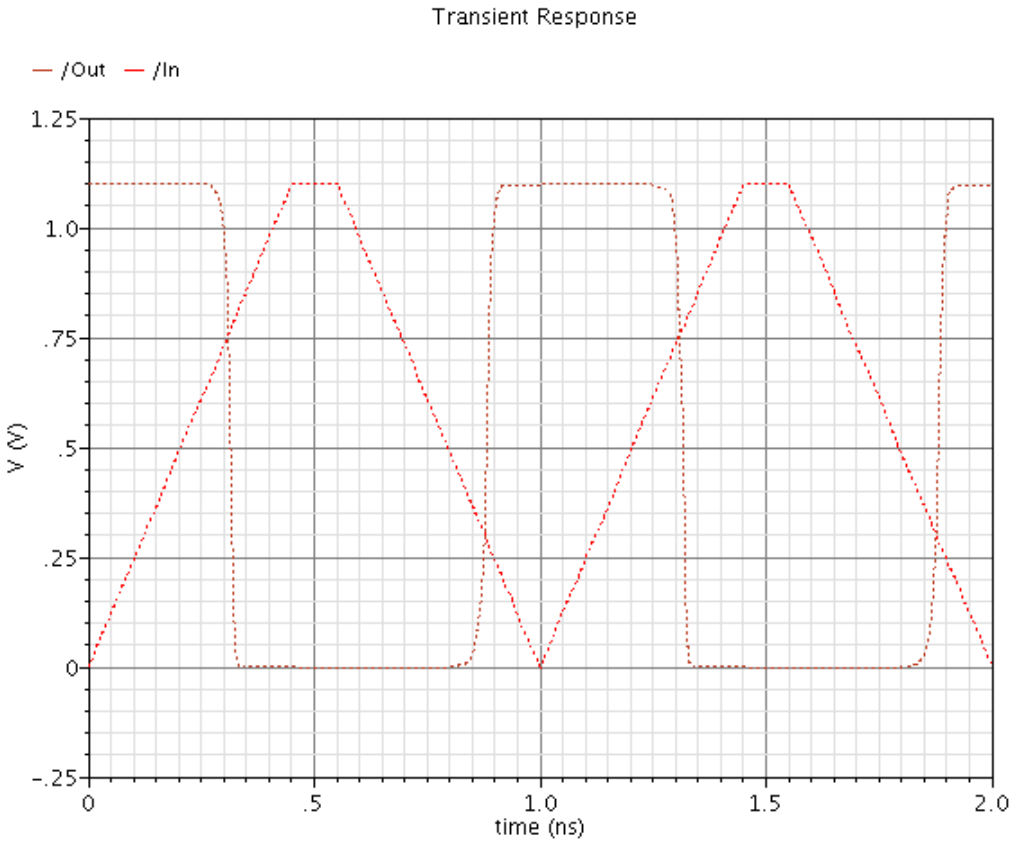
The paper described by section 2.1 proposes a timer that uses the following components:

1. Schmitt Trigger.
2. Inverter.
3. Leakage-based current Source with a huge capacitance.

3.1. Schmitt Trigger

The Schmitt trigger displays different switching thresholds called V_{M+} and V_{M-}. In the graphs below, the schematic proposed in the paper (section 2.1) and the simulation using a triangular waveform as the input. For this particular simulation V_{M+} and V_{M-} are around 0.75V and 0.25V.

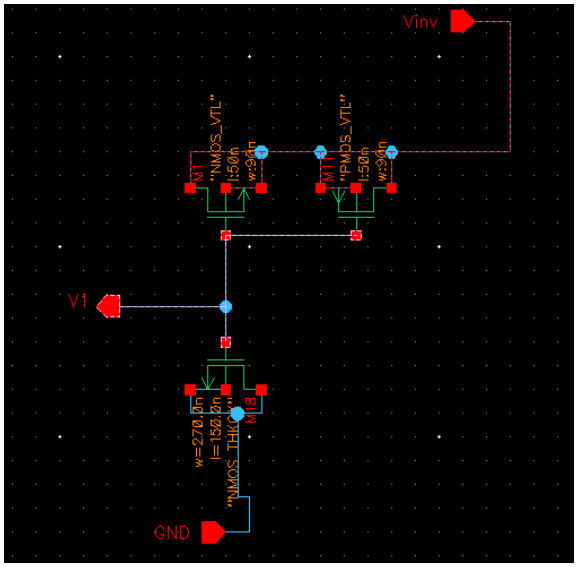


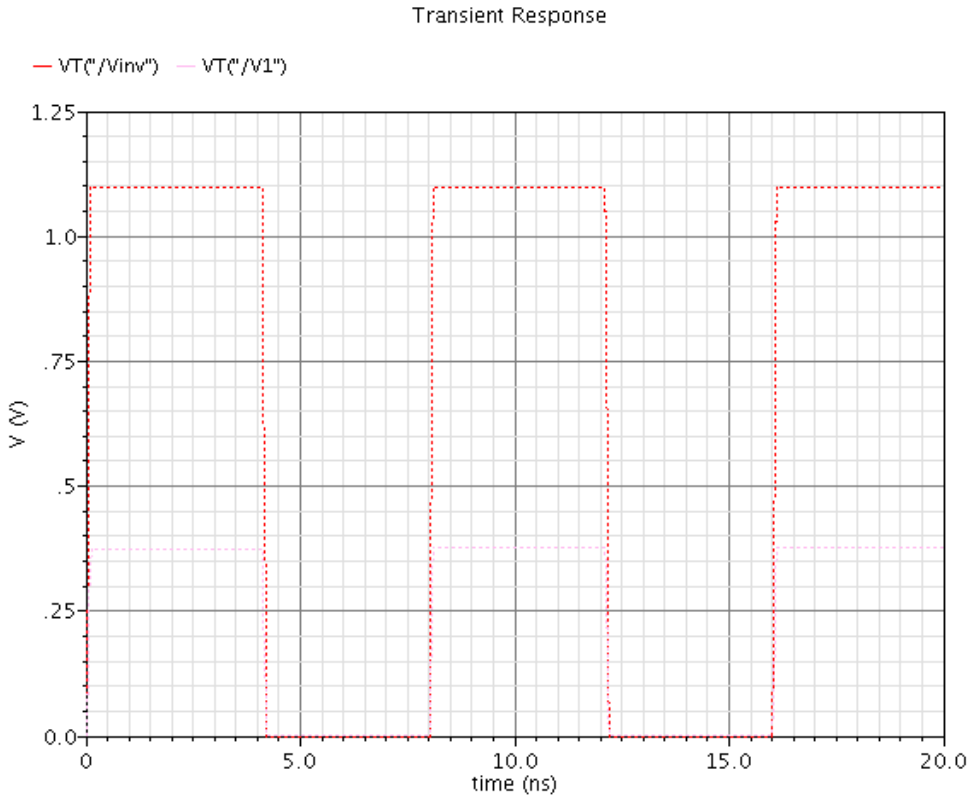


In the following sections we show simulation results of the Schmitt Trigger and the leakage based current source using spectre.

3.2. Current Source

The graphics below show the current source schematic and the transient simulation.





We vary the size of the transistor to vary the gate capacitance and got the following voltage variation.

Transistor Size	Voltage at the input of the Schmitt Trigger.
270n	376m
720nm	186m

Bibliography

[1] Y.-S. Lin, D. Sylvester, and D. Blaauw, "A Sub-pW Timer Using Gate Leakage for Ultra Low-Power Sub-Hz Monitoring Systems," IEEE Custom Integrated Circuits Conference, 2007
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[3] Y. Lee, B. Giridhar, Z. Foo, D. Sylvester, D. Blaauw, "A 660pW Multi-stage Temperature Compensated Timer for Ultra-low Power Wireless Sensor Node Synchronization", IEEE International Solid State Circuits Conference, 2011.
[4] B. Zhai, L. Nazhandali, J. Olson et al., "A 2.60 pJ/inst subthreshold sensor processor for optimal energy efficiency," in Proceedings of the IEEE Symposium on VLSI Circuits, Digest of Technical Papers (VLSIC '06), pp. 154–155, June 2006.
[5] S.M. Pernia, J.D. O'Day, G.Carichner et al., "A 0.5–480MHz Self-Referenced CMOS Clock Generator with 90ppm Total Frequency Error and Spread Spectrum Capability," *IEEE International Solid State Circuits Conference* (*ISSCC*) *Dig. of Tech. Papers*, Feb. 2008
[6] B. Zhai, S. Hanson, D. Blaauw, and D. Sylvester, "Analysis and mitigation of variability in subthreshold design," in Proc. International Symposium on Low Power Electronics and Design (ISLPED), 2005